ABSTRACT OF THE DISCLOSURE

The interface between a trench isolation layer and a semiconductor substrate at the uppermost part of the trench isolation region has a curvilinear sectional profile to prevent an electric field from concentrating at the upper corners of the substrate where the active regions are formed. A pad oxide layer and a hard mask layer are sequentially formed on the semiconductor substrate, and are then patterned using photolithography to form a hard mask pattern and a pad oxide pattern. Subsequently, a thermal oxide layer is formed on the substrate, either directly thereon or in a shallow trench formed therein. The thermal oxide layer and the semiconductor substrate are then etched using the hard mask pattern as a mask to form a deep trench and yet leave an outer peripheral portion of the thermal oxide layer at the upper part of the trench isolation region. A buffer layer is formed over the entire upper stepped surface of the resulting structure and then the deep trench is filled with an oxide layer. The resulting structure is planarized and the hard mask pattern is removed to thereby complete the formation of the trench isolation layer.